Abstract

According to the present invention, an overlay margin is secured for matching a wiring electrode 11 with a storage electrode 15 of a capacitor at their point of contact and the required area for a memory cell can be decreased by placing the plug electrode 11 of titanium nitride in the active region of a semiconductor substrate or over the gate electrode, reducing the size of the opening for passing the storage electrode 15 of the capacitor of a stacked structure, and decreasing the line width of a wiring electrode 13. By the common use of the above-mentioned plug electrodes in a CMISFET region in the peripheral circuit and in a memory cell of a static RAM, their circuit layouts can be made compact.